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09/731,697	12/08/2000	Kenji Matsumura	FQ5-510	9688

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EXAMINER	
WILSON, ROBERT W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/731,697	Applicant(s) MATSUMURA, KENJI	
	Examiner Robert W Wilson	Art Unit 2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.0 The application of Kenji Matsumura entitled "MULTI-RATE ATM SWITCHING SYSTEM AND METHOD" filed on 12/8/2000 with a request for foreign priority based upon JAPAN 350778/1999 12/09/1999 was examined. Claims 1-16 are pending.

Claim Rejections - 35 USC § 112

2.0 The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-8 & 13-16 are rejected because the metes and the bounds of the claims cannot be assessed.

Referring to **Claim 4**, Please note that Claim 4 depends on Claim 1 only and claim 1 does not introduce the concept of a First FIFO. The applicant introduces the concept of a 2nd FIFO but does not make it clear how the second FIFO fits into the architecture. What is meant by a 2nd FIFO? What is second FIFO connected between? Is the second FIFO connected between the first FIFO and the ATM CORE SWITCH?

Referring to **Claim 5**, Please note that Claim 5 depends upon Claims 3, 2, & 1 respectively. The applicant introduces the concept of a 2nd FIFO but does not make in clear as to how the 2nd FIFO is interconnected into the architecture. What is meant by a second FIFO? Is the second FIFO interconnected between the first FIFO and the ATM CORE SWITCH?

Referring to **Claim 6**, Please note that Claim 6 depends upon claims 3,2, & 1 respectively. The applicant has introduced the concept of a 1st sequence selector but not made it clear how the 1st sequence selector is connected into the architecture. Is the 1st sequence selector between the input port and the first selector?

Referring to **Claim 7**, Please note that Claim 7 depends upon claims 6,3,2, &1 respectively. The concept of a 3rd FIFO has been introduced by the applicant; however the concept of a 2nd FIFO has not yet been introduced. What is meant by "3rd FIFO"? Is the 3rd FIFO interconnected between the Switch Core and the 2nd Selector?

Referring to **Claim 8**, Please note that Claim 8 depends upon claims 7, 6, 3, 2, & 1 respectively. The concept of a 3rd FIFO has been introduced by the applicant; however the concept of a 2nd FIFO has not yet been introduced in the dependent claims. What is meant by "3rd FIFO"? Is the 3rd FIFO interconnected between the Switch Core and the 2nd Selector?

Referring to **Claim 12,** Please note that Claim 12 depends upon Claim 9. Claim 9 does not introduced the concept of a 1st FIFO. What is meant by a 2nd FIFO; furthermore, it is not clear from the claim how the 2nd FIFO is connected into the architecture.

Referring to **Claim 13**, Please note that Claim 13 depends upon claims 11, 10, & 9 respectively. These dependent claims do not introduced the concept of a 1st FIFO but introduces the concept of a FIFO. What is meant by a 2nd FIFO; furthermore, it is not clear from the claim how the 2nd FIFO and the switching function are connected into the architecture.

Referring to **Claim 14**, Please note that Claim 14 depends upon claims 10 & 9 respectively. The applicant introduces the concept of "sequence id function" but does not specify where in the architecture the function is performed. Is the Sequence Id function performed between the Input port and the selector?

Referring to **Claim 15**, Please note that claim 15 depends upon claims 11, 10, & 9. The applicant introduces the concept of a 3rd FIFO when the concept of a First and second FIFO have not been introduced. What is meant by a 3rd FIFO? How does the 3rd FIFO fit into the architecture? Is the third FIFO between the switch core and the MUX?

Referring to **Claim 16**, Please note that claim 16 depends upon claims 15, 11, 10, & 9. The applicant introduces the concept of the 2nd FIFO and switch function but does not specify how they fit into the overall architecture. What is meant by a 2nd FIFO and switch function? It should also be noted that the applicant has only introduce the concept of a FIFO and not a First FIFO in the dependent claims also.

Claim Rejections - 35 USC § 103

3.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozaki et. al. (U.S. Patent No.: 5,099,475 which is an IDS document of record).

Referring to **Claim 1**, Kozaki teaches: A multi-rate switching system (Fig 1) comprising:

An ATM (asynchronous transfer mode) switch having a plurality of input and output ports each having different port numbers assigned thereto (Fig 1 shows a cell or ATM switch which has input ports #A & #B and output ports #a & #b which are numbered differently);

Wherein the ATM cells arriving at respective one of the input ports are transferred to appropriate ones of the output ports in units of a predetermined time period based on header information of each of the ATM cells (Fig 1 shows that the header is read by 21 or 22. The applicant broadly claims "predetermined time".):

A cell demultiplexer for distributing a flow of incoming ATM cells in units of an ATM cell to a plurality of predetermined input ports of the ATM switch in an order in which the incoming ATM cells arrive (Fig 1 shows the flow of incoming cells or ATM cells where demultiplexing is performed in 31 or 32);

A cell multiplexer for multiplexing outgoing ATM cells received in parallel from a plurality of predetermined output ports of the ATM switch to product a flow of outgoing ATM cells (Fig 1 shows 71 or 72 which perform the multiplexing)

Kozaki does not expressly call for: predetermined time but teaches that there are functions perform in a specific order per Fig 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention that functions performed in a specific order results in a time duration which can be predetermined.

In Addition:

Regarding **Claim 2**, wherein the cell demultiplexer comprises: a first selector for sequentially selecting parallel lines in a predetermined order of the parallel lines to output an incoming ATM cell to a selected one of the parallel lines, wherein the parallel lines correspond to the predetermined input ports of the ATM switch (It would have been obvious to one of ordinary skill in the art at the time of the invention that in addition to performing the demultiplexing that 31 or 32 sequentially select parallel lines in a predetermined order in order for the invention to work)

A first FIFO buffer for temporarily storing incoming ATM cells received through the parallel lines from the first selector in a first-in-first out (FIFO) scheme to output them in parallel to the predetermined input ports of the ATM switch in synchronization with each other (BFMLSI 40 per Fig 1 or first FIFO)

Regarding **Claim 3**, a second selector for sequentially selecting one of the outgoing ATM cells in a predetermined order of the predetermined output ports to produce the flow of the outgoing ATM cells (71 or 72 per Fig 1 or second selector)

Regarding **Claim 4**, wherein the ATM switch comprises:

A second FIFO buffer for temporarily storing ATM cells to be transferred to respective ones of the input ports in a FIFO scheme (61 & BFM LSI 40 per fig 1 perform the same function as the second FIFO)

A switch controller for controlling cell switching of a plurality of ATM cells to be forward to the predetermined output ports such that the plurality of ATM cells to be forwarded to the predetermined output ports are sequentially assigned to sequential ones of the predetermined output ports in a circular manner (data is output one after another into RT DEC per Fig 1 or per col. 7 lines 36-40 or switch controller)

An ATM switch core for switching the ATM cells stored in the second FIFO buffer under cell switching control of the switch controller (RT DEC or switch core per Fig 1)

Regarding **Claim 5**, wherein the ATM switch comprises: a second FIFO buffer for temporarily storing ATM cells to be transferred to respective ones of the input ports in a FIFO scheme (61 & BFMLSI 40 which perform the function of the second FIFO)

A switch controller for controlling cell switching of plurality of ATM cells to be forwarded to the predetermined output ports such that the plurality of ATM cells to be forwarded to the predetermined output ports are sequentially assigned to sequential ones of the predetermined output ports in a circular manner (data is output one after another into RT DEC per Fig 1 or per col. 7 lines 36-40 or switch controller. Data is output sequentially in a per col. 7 line 65-col. 8 line 15)

An ATM switch core for switching the ATM cells stored in the second FIFO buffer under cell switching control of the switch controller (RT DEC or switch core per Fig 1)

Regarding **Claim 6**, wherein the cell demultiplexer further comprises: a first sequence controller for providing each of the incoming ATM cells with a sequence identification number indicating an arrival order thereof, wherein the incoming ATM cells with sequence identification numbers are transferred to the first selector (31 or 32 perform the function of first sequence controller because they put the cells in a sequence as shown in Fig 1. 31 or 32 are the first selector)

Regarding **Claim 7**, wherein the cell multiplexer further comprises: a third FIFO buffer for temporarily storing the outgoing ATM cells in a FIFO scheme (BFM LSI 40 & 532 perform the function of third FIFO per Fig 1)

A second sequence controller for determining whether the outgoing ATM cells stored in the third FIFO buffer are in order by checking the sequence identification numbers of the outgoing ATM cells (OUT DEC per Fig 1 or second sequence controller)

Regarding **Claim 8**, wherein the ATM switch comprises: a second FIFO buffer for temporarily storing ATM cells to be transferred to respective ones of the input ports in a FIFO scheme (61 & BFM LSI 40 perform the function of second FIFO per Fig 1)

A switch controller for controlling cell switching of a plurality of ATM cells to be forwarded to the predetermined output ports such that the plurality of ATM cells to be forwarded to the predetermined output ports are sequentially assigned to sequential ones of the predetermined output ports in a circular manner (data is output one after another into RT DEC per Fig 1 or per col. 7 lines 36-40 or switch controller. Data is output sequentially in a per col. 7 line 65-col. 8 line 15)

Referring to **Claim 9**, Kozaki teaches: The multi-rate switching method (Fig 1) using an ATM (asynchronous transfer mode) switching having a plurality of input output ports each having different port numbers assigned thereto (Fig 1 shows a cell or ATM switch which has input ports #A & #B and output ports #a & #b which are numbered differently);
Wherein ATM cells arriving at respective one of the input ports are transferred to appropriate ones of the output ports in units of predetermined time period based on header information of each of the ATM cells (Fig 1 shows that the header is read by 21 or 22 prior and eventually the cells are transferred to the output ports. The applicant broadly claims "predetermined time".)

a) distributing a flow of incoming ATM cells in units of an ATM cell to a plurality of predetermined input ports of the ATM switch in an order in which the incoming ATM cells arrived (Fig 1 shows distributing incoming cells or ATM cells to a plurality of input ports)

b) multiplexing outgoing ATM cells received in parallel from a plurality of predetermined output ports of the ATM switch to product a flow of outgoing ATM cells (71 or 72 multiplex parallel flows of cells or ATM cells)

Kozaki does not expressly call for: predetermined time but teaches that there are functions perform in a specific order per Fig 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention that functions performed in a specific order results in a time duration which can be predetermined.

In Addition:

Regarding **Claim 10**, wherein the step (a) comprises the steps of :

a.1) sequentially selecting parallel lines in a predetermined order of the parallel lines to output an incoming ATM cell to a selected one of the parallel lines, wherein the parallel lines correspond to the predetermined input ports of the ATM switch (31 or 32 or selecting per Fig 1) and;

a.2) temporarily storing incoming ATM cells received through the parallel lines in a first FIFO (first-in-first-out) buffer to output them in parallel to the predetermined input ports of the ATM switch in synchronization with each other (BFMLSI 40 per fig 1 or first FIFO)

Regarding **Claim 11**, wherein the step (b) comprises the step of:

b.1) sequentially selecting one of the outgoing ATM cells in a predetermined order of the predetermined output ports to produce the flow of the outgoing ATM cells (71 or 72 per Fig 1)

Regarding **Claim 12**, further comprising the steps of: at the ATM switch, temporarily storing ATM cells to be transferred to respective ones of the input ports in a second FIFO buffer (61 & BFMLSI 40 perform the function of the second FIFO per Fig 1)

Controlling cell switching of a plurality of ATM cells to be forwarded to the predetermined output ports such that the plurality of ATM cells to be forwarded to the predetermined output ports are sequentially assigned to sequential ones of the predetermined output ports in a circular manner (71 or 72 per Fig 1 sequentially select)

Regarding **Claim 13**, further comprising the steps of:
At the ATM switch, temporarily storing ATM cells to be transferred to the respective ones of the input ports in a second FIFO buffer (61 & BFMI LSI 40 perform the function of the 2nd FIFO per Fig 1)

Controlling cell switching of a plurality of ATM cells to be forwarded to the predetermined output ports such that the plurality of ATM cells to be forwarded to the predetermined output ports are sequentially assigned to sequential ones of the predetermined output ports in a circular manner (OUT DEC per Fig 1 or output sequence controller)

Switching the ATM cells stored in the second FIFO buffer under control of the cell switching (RT DEC or switching per Fig 1)

Regarding **Claim 14**, wherein the step (a) further comprises the step of:

A.0) providing each of the incoming ATM cells with a sequence identification number indicating an arrival order thereof, wherein the incoming ATM cells with a sequence identification numbers are used at step (a.1) (31 or 32 perform the function of first sequencing because they put the cells in a sequence as shown in Fig 1. It would have been obvious to one of ordinary skill in the art at the time of the invention that they would be assigned sequence numbers in order for the invention to work)

Regarding **Claim 15**, wherein the step (b) further comprises the steps of:

Temporarily storing the outgoing ATM cells in a third FIFO buffer (BFMLSI 40 and 52 perform the same function as a 3rd FIFO buffer)

Determining whether the outgoing ATM cells stored in the third FIFO buffer are in order by checking the sequence identification numbers of the outgoing ATM cells (Function performed between 71 and #a per Fig 1. It would have been obvious to one of ordinary skill in the art at the time of the invention that this function is performed in order for the invention to work)

When the outgoing ATM cells are not in order, controlling the third FIFO buffer such that the outgoing ATM cells are read out from the third FIFO buffer in the order of sequence identification numbers (Function performed between 71 and #a per Fig 1. It would have been obvious to one of ordinary skill in the art at the time of the invention that this function is performed in order for the invention to work)

Regarding **Claim 16**, further comprising the steps of: at the ATM switch, temporarily storing ATM cells to be transferred to respective ones of the input ports in a second FIFO buffer (61 & BFMI LSI 40 perform the function of the 2nd FIFO per Fig 1)

Controlling cell switching of a plurality of ATM cells to be forwarded to the predetermined output ports such that the plurality of ATM cells to be forwarded to the predetermined output ports are sequentially assigned to sequential ones of the predetermined output ports in a circular manner (OUT DEC per Fig 1 or output sequence controller)

Switching the ATM cells stored in the second FIF buffer under control of the cell switching (RT DEC or switching per Fig 1)

Conclusion

4.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is (703) 305-4703. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
June 16, 2004